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10/693,191	10/23/2003	Toru Ishikawa	P/126-223	2324

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EXAMINER	
WEINMAN, SEAN M	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,191	ISHIKAWA, TORU	
	Examiner	Art Unit	
	Sean Weinman	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 and 4-9 is/are rejected.

7)☒ Claim(s) 2 and 3 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/30/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 are presented for examination

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claims 4-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims 4 recites "a circuit" on page 16 line 20. It is unclear whether this is intended to be the same as or different from the "circuit" recited on page 15 line 11. Additionally, claim 4 recites "an internal clock signal" on page 16 lines 20-21. It is unclear whether this is intended to be the same as or different from the "internal clock signal" recited on page 15 line 8.

5. Claim 5 recites "a delay time" on page 16 line 25 and also on lines 25-26. It is unclear whether this is intended to be the same as or different from the "delay time" recited on page 16 lines 16-17. Additionally, claim 5 recites "a register" on page 16 line 25. It is unclear whether this is intended to be the same as or different from the "register" recited on page 16 line 17. Additionally, claim 5 recites "a content" on page 16 line 25. It is unclear whether this is intended to be the same as or different from the "content" recited on page 16 line 17. Additionally, claim 5 recites "a fuse" on page 16 line 26. It is unclear whether this is intended to be the same as or different from the "fuse" recited on page 16 line 17. Additionally, claim 5, recites "a circuit" on page 16 line

28. It is unclear whether this is intended to be the same as or different from the "circuit" recited on page 15 line 11. Additionally, claim 5 recites "an internal clock signal" on page 16 line 28. It is unclear whether this is intended to be the same as or different from the "internal clock signal" recited on page 15 line 8.

6. Claim 6 recites the limitation "the delay time" on page 17 line 8. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 8 recites "a data input circuit" on page 17 line 23. It is unclear whether this is intended to be the same as or different from the "data input circuit" on page 17 line 9. Additionally, claim 8 recites "a circuit" on page 17 line 24. It is unclear whether this is intended to be the same as or different from the "circuit" recited on page 15 line 11. Additionally, claim 8 recites "an internal clock signal" on page 17 line 25. It is unclear whether this is intended to be the same as or different from the "internal clock signal" recited on page 15 line 8.

8. Claim 9 recites "a delay time" on page 17 line 29. It is unclear whether this is intended to be the same as or different from the "delay time" recited on page 17 line 8. Additionally, claim 9 recites "a content" on page 17 line 29. It is unclear whether this is intended to be the same as or different from the "content" recited on page 17 line 19. Additionally, claim 9 recites "a register" on page 17 line 29. It is unclear whether this is intended to be the same as or different from the "register" recited on page 17 line 19. Additionally, claim 9 recites "a fuse" on page 18 line 1. It is unclear whether this is intended to be the same as or different from the "fuse" recited on page 17 line 120. Additionally, claim 9, recites "a circuit" on page 18 line 3. It is unclear whether this is

intended to be the same as or different from the "circuit" recited on page 15 line 11. Additionally, claim 9 recites "an internal clock signal" on page 18 line 4. It is unclear whether this is intended to be the same as or different from the "internal clock signal" recited on page 15 line 8.

9. Any claim not specifically addressed, above, is being rejected as incorporating the deficiencies of a claim upon which it depends.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1, 4, and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission of Prior Art (AAPA) , and in further view of Dortu (US Patent No. 6,043,694).

12. As per claim 1, the AAPA teaches the invention comprising:

an input circuit for outputting an external clock signal (Figure 1 Reference character 52 and Paragraph [0006]);

a delay adjustment circuit for delaying the input clock signal (Figure 1 Reference character 53 and Paragraph [0006]);

a clock driver for outputting an internal clock signal in response to the delayed input clock signal from the delay adjustment circuit (Figure 1 Reference character 54 and Paragraph [0006]),

the timing adjustment circuit further comprising a phase advance/delay signal generation unit for using the internal clock signal and e the external clock signal to produce a phase advance/delay signal indicating whether the phase of the output signal from the circuit to be driven advances or delays with respect to the phase of the external clock signal (Figure 1 Reference character 57 and 58 and Paragraphs [0006] and [0007]).

13. The AAPA does not teach a phase advance/delay signal generation unit using the internal clock with the external clock and the output signal from the circuit to produce a phase advance/delay signal. Specifically, the AAPA teaches a timing adjustment circuit which comprises a input circuit for outputting an external clock, a delay adjustment circuit for delaying the input clock signal, a clock driver for outputting an internal clock signal in response to the delayed input clock signal, and a phase advance/delay signal generation unit for using the internal clock signal with the external clock signal to produce a phase advance/delay signal. The AAPA does not teach that the phase advance/delay signal generation unit uses the output signal from the circuit to be driven.

14. Dortu teaches a timing adjustment circuit in which the output signal from the data circuit is fed back to a phase comparison circuit to produce a control signal for indicating the phase relationship of the signals. Dortu teaches using the internal clock signal the output signal of the circuit to be driven to produce a phase advance/delay signal indicating whether the phase of the output signal from the circuit to be driven advances or delays with respect to the phase of the external clock signal (Col. 5 lines 5-8 and

lines 23-34 and Figure 1 Reference characters 24, 28 and 30). Specifically, Dortu teaches a timing adjustment circuit having a phase advance/delay signal generation unit, which uses the output signal from the circuit and the input clock to produce a signal indicating and used to adjust the signals and their phase relationship.

15. It would have been obvious to one of ordinary skill in the art to combine the teachings of the AAPA and Dortu because they both teach timing adjustment circuits having a phase advance/delay signal generation circuit to produce a control signal indicating the signals are in phase and to adjust the phase according to their relationship. Dortu covers the deficiency of the AAPA by teaching the phase advance/delay signal generation unit using the output signal from the driven circuit along with the input clock to produce a signal indicating the phase relationship between the input clock signal and output signal.

16. As per claim 4, the AAPA teaches the invention comprising:

a data output circuit for functioning as a circuit to be driven by an internal clock signal supplied from the timing adjustment circuit to output data at a timing defined by the internal clock signal (Figure 1 Reference character 55 and Paragraph [0007]).

17. As per claim 6, the AAPA teaches the invention comprising:

the delay adjustment circuit is constituted to be capable of changing the delay time, the circuit to be driven is a data input circuit for latching input data supplied from the outside in synchronization with the internal clock signal, and the phase advance/delay signal generation unit includes the same constitution as that of the circuit to be driven and comprises a unit for receiving supply of the external clock signal

instead of the input data to latch the external clock signal in synchronization with the internal clock signal and for outputting the phase advance/delay signal to the outside (Figure 2 Reference characters 60, 61, 63, 64 and 66 and Paragraphs [0015]-[0020]).

18. As per claim 7, the AAPA teaches the invention comprising:

the delay adjustment circuit is constituted to be capable of adjusting the delay time by change of a content held by a register or by disconnection of a fuse (Paragraph [0013]).

19. As per claim 8, the AAPA teaches the invention comprising:

a data input circuit for latching input data supplied from the outside at a timing defined by the internal clock signal, which is a circuit to be driven by an internal clock signal supplied from the timing adjustment circuit (Figure 2 Reference character 66 and Paragraphs [0015] and [0017]).

20. As per claim 9, the AAPA teaches the invention comprising:

the timing adjustment circuit according to claim 7 capable of adjusting both a delay time by change of a content held by a register and a delay time by disconnection of a fuse; and a data input circuit for latching input data supplied from the outside at a timing defined by the internal clock signal, which is a circuit to be driven by an internal clock signal supplied from the timing adjustment circuit, wherein a tester connected to the phase advance/delay signal generation unit is used to monitor the phase advance/delay signal while the content held by the register is changed to obtain an appropriate delay time, and subsequently the fuse is disconnected so that the delay

time of the timing adjustment circuit can be fixed to the appropriate delay time. (Figure 2 Reference characters 60, 61, 63, 64 and 66 and Paragraphs [0015] – [0020]).

21. Claims 2, 3, and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Weinman whose phone number is (571) 272-2744. The examiner can normally be reached on Monday-Friday from 8:00-4:30.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sean Weinman
Examiner
Art Unit 2115

CHUN CAO
PRIMARY EXAMINER